ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS
(MR13 Regulations)

For

M.Tech. (VLSI SYSTEM DESIGN)
(Applicable for the batches admitted from academic year 2013-14)

Department of Electrical & Electronics Engineering
MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

Maisammaguda, Dulapally (post & via Kompally), Secunderabsd-500 100
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MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

Maisammaguda, Dhulapally (Post via. Kompally), Secunderabad – 500100

ACADEMIC REGULATIONS MR 13 FOR M. TECH. (REGULAR) DEGREE COURSE

(Effective for the students admitted into first year from the academic year 2013-2014)

The M.Tech Degree of Malla Reddy Engineering College, Hyderabad shall be conferred on candidates by the Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to the eligibility, qualifications and Specialization as prescribed by the university/college from time to time.

Admissions shall be made on the basis of merit/rank obtained by the qualifying candidate at an Entrance Test conducted by the University/college or on the basis of any other order of merit approved by the University/college (say **PGECET/GATE)** subject to reservations as laid down by the Government from time to time.

2.0 AWARD OF M. TECH. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four Academic years from the year of his admission, shall forfeit his seat inM. Tech. course.

2.3 The student shall register for all 88 credits and secure all the 88 credits.

2.4 The minimum instruction days in each semester are 90.

3.0 A. COURSES OF STUDY

The following specializations are offered at present for the M. Tech. course of study.

1. Advanced Manufacturing Systems(AMS) - Shift II
2. Computer Science(CS) - Shift I
3. Computer Science and Engineering(CSE) - Shift I & II
4. Control Engineering(CE) - Shift I
5. Control Systems(CS) - Shift I & II
6. Digital Systems and Computer Electronics(DSCE) - Shift I & II
7. Embedded Systems(ES) - Shift I
8. Geotechnical Engineering(GTE) - Shift I
9. Power Electronics and Electrical Drives(PEED) - Shift II
10. Structural Engineering(SE) - Shift I
11. Transportation Engineering(TE) - Shift II
12. Thermal Engineering(THE) - Shift I
13. VLSI System Design(VLSI SD) - Shift I

3.0 B. Departments offering M. Tech. Programmes with specializations are noted below:

Civil Engineering Department.	1. Structural Engineering(SE) 2. Transportation Engineering(TE) 3. Geotechnical Engineering(GTE)
Computer Science & Engineering Department	1. Computer Science(CS) 2. Computer Science and Engineering(CSE)
Electrical & Electronics Engineering Department	1. Control Systems(CS) 2. Control Engineering(CE) 3. Power Electronics and Electrical Drives(PEED)
Electronics & Communication Engineering Department	1.Digital Systems and Computer Electronics(DSCE) 2. VLSI System Design(VLSI SD) 3. Embedded Systems(ES)
Mechanical Engineering Department	1. Thermal Engineering(THE) 2. Advanced Manufacturing Systems(AMS)

4.0 ATTENDANCE

The programs are offered on a unit basis with each subject being considered a unit.

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class and their registration shall stand cancelled.

4.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

4.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the previous semester including the days of attendance in sports, games, NCC and NSS activities.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 75 marks shall be awarded based on the performance in the End Semester Examination and 25 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for a total duration of 120 minutes with Part A as one question to be answered out of two questions, which carries 10 marks and Part B with 3 questions to be answered out of 5 questions each question for 5 marks. If any candidate is absent for any subject of a mid -term examination, an additional exam will be conducted in the deserving cases based on the recommendations of the College Academic Committee. End semester examination is conducted for 75 marks with 5 questions to be answered out of 8 questions, each question carries 15 marks.

5.2 For practical subjects, 75 marks shall be awarded based on the performance in the End Semester Examinations and 25 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is intended to assess the students' understanding of various subjects he has studied during the M. Tech. course of study. The Comprehensive Viva-Voce is evaluated for 100 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.5) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be another Laboratory Teacher.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation after taking up a topic approved by the Project Review Committee(PRC).

6.1 A Project Review Committee shall be constituted with Principal as chair person, Head of the Department, Coordinator, Supervisor and two other senior faculty members.

6.2Registration of Project Work: A candidate is permitted to register for the project work after satisfyingthe attendance requirement of all the subjects (theory and practical subjects).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Academic Committee for its approval. Only after obtaining the approval of the Departmental Academic Committee can the student initiate the Project work.Departmental Committee(DAC) Consists of Head of the Department as Chairman, along with two Senior Professors and few subject experts too.

6.4 If a candidate wishes to change his supervisor or topic of the project he can do so with approval of Departmental Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of topic as the case may be.

6.5 Candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation/demonstration before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the College. For this, Head of the Department shall submit a panel of 3 examiners to the Chief Controller of Examinations of the College, who are eminent in that field with the help of the concerned guide and Head of the department.

6.9 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as described by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work as one of the following:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva- Voce examination.

If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, he will not be eligible for the award of the degree unless he is asked to revise and resubmit by the Board.

7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the programand is eligible for the award of M. Tech. Degree he shall be placed in one of the followingfour classes:

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70 but not less than 60%
Second Class	Below 60% but not less than 50%
Pass Class	Below 50% but not less than 40%

The marks in internal evaluation and end examination shall be shown separately in thememorandum of marks.

8.0WITH-HOLDING OF RESULTS

If the candidate has not paid any dues to the university or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS

9.1 Discontinued, detained or failed candidates are eligible for admission to two earlier orequivalent subjects at a time as and when offered.
9.2 The candidate who fails in any subject will be given two chances to pass the same subject:otherwise, he has to identify an equivalent subject as per MR13 academic regulations.

10.0GENERAL

10.1The academic regulations should be read as a whole for purpose of any interpretation.
10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision ofthe Principal is final.
10.3The College may change or amend the academic regulations and syllabus at any time andthe changes and amendments made shall be applicable to all the students with effect from thedate notified by the College.
10.4Wherever the word he, him or his occur, it will also include she, her and hers.
10.5 Wherever the word 'Subject' occurs in the above regulations, it implies the 'Theory Subject' and'Practical Subject' or 'Lab'.
10.5Transfers not allowed among group colleges.

MALPRACTICES RULES
DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any mark son the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shallot be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject tithe academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject

6	Refuses to obey the orders of the Chief Superintendent/Assistant –Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to the person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-incharge,or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police cases registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.

12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action toward suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)

(i) A show cause notice shall be issued to the college.
(ii) Impose a suitable fine on the college.
(iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)
M.Tech. (VLSI SYSTEM DESIGN)
COURSE STRUCTURE AND DETAILED SYLLABUS
(MR13 Regulations)

I Year- I Semester

Code	Group	Subject	L	P	Credits
MR134101	**Core**	VLSI technology & design	3	0	3
MR134201	**Core**	CMOS analog integrated circuit design	3	0	3
MR134115	**Core**	CPLD & FPGA architectures and applications	3	0	3
MR134108	**Core**	CMOS digital integrated circuit design	3	0	3
MR134102 MR134202 MR134203	**Elective I**	Digital System Design Hardware Software Co-Design Device Modeling	3	0	3
MR135103 MR134104 MR135130	**Elective II**	Advanced Operating Systems Micro controllers for embedded system design Advanced Computer Architecture	3	0	3
MR134204	**Lab**	VLSI System Design Lab I	0	2	2
MR134210		Seminar	-	-	2
		Total Credits			22

I Year- II Semester

Code	Group	Subject	L	P	Credits
MR134111	**Core**	Low power VLSI design	3	0	3
MR134205	**Core**	CAD for VLSI Circuits	3	0	3
MR134116	**Core**	CMOS mixed signal circuit design	3	0	3
MR134112	**Core**	Design for testability	3	0	3
MR135132 MR134117 MR134206	**Elective III**	Scripting Languages Digital signal processors and architectures VLSI Signal Processing	3	0	3
MR134207 MR134115 MR134208	**Elective IV**	Optimization Techniques in VLSI design System on chip architecture Semi Conductor memory design and testing	3	0	3
MR134209	**Lab**	Mixed signal Design Lab	0	2	2
MR134220		Seminar	-	-	2
		Total Credits			22

II Year – I & II Semester

CODE	Subject	L	P	Credits
MR134221	Comprehensive Viva	-	-	4
MR134222	Project work and Seminar	-	-	40
	Total	-	-	44

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

VLSI TECHNOLOGY AND DESIGN

UNIT –I:

REVIEWOF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES:MOS, CMOS, BiCMOSTechnology.Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, ThresholdVoltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOSTransistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES &LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive andInductive interconnect delays.

UNIT –III:

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks,Gate and Network testing.

UNIT –IV:

SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Designvalidation andtesting.

UNIT –V:

FLOOR PLANNING: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. EshraghianEshraghian. D, A. Pucknell, 2005,PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT -I:
MOS DEVICES AND MODELING: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOSDevice Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model forthe MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:
ANALOG CMOS SUB-CIRCUITS:MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Currentmirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current andVoltage References, Band gap Reference.

UNIT -III:
CMOS AMPLIFIERS: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High GainAmplifiers Architectures.

UNIT -IV:
CMOS OPERATIONAL AMPLIFIERS: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, PowerSupply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp.

UNIT -V:
COMPARATORS: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-LoopComparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:
1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:
1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:
INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable LogicArrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; ComplexProgrammable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLDImplementation of a Parallel Adder with Accumulation.

UNIT-II:
FIELD PROGRAMMABLE GATE ARRAYS: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures,Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated SpecializedComponents of FPGAs, Applications of FPGAs.

UNIT -III:
SRAM PROGRAMMABLE FPGAS: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.

UNIT -IV:
ANTI-FUSE PROGRAMMED FPGAS: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3Architectures.

UNIT -V:
DESIGN APPLICATIONS: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a RobotManipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders andAccumulators with the ACT Architecture.

TEXT BOOKS:
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

UNIT –I:
MOS DESIGN: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage,Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates,Transistor equivalency, CMOS Inverter logic.

UNIT –II:
COMBINATIONAL MOS LOGIC CIRCUITS:MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, ComplexLogic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI andOIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
SEQUENTIAL MOS LOGIC CIRCUITS: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edgetriggered flipflop.

UNIT –IV:
DYNAMIC LOGIC CIRCUITS:Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOStransmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
SEMICONDUCTOR MEMORIES:Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell andrefresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash andNAND flash.

TEXT BOOKS:
1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

DIGITAL SYSTEM DESIGN
(Elective-I)

UNIT -I:
MINIMIZATION AND TRANSFORMATION OF SEQUENTIAL MACHINES: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machineminimization – Simplification of incompletely specified machines.Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cyclesand Hazards.

UNIT -II:
DIGITAL DESIGN: Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for controlcircuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner,inary divider.

UNIT -III:
SM CHARTS: State machine charts, Derivation of SM Charts, Realization of SM Chart, implementation of BinaryMultiplier, dice game controller.

UNIT -IV:
FAULT MODELING & TEST PATTERN GENERATION: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Faultdominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques,Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Randomtesting, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:
FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: Circuit Test Approach, Transition Check Approach – State identification and fault detectionexperiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A.
Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:
1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

HARDWARE - SOFTWARE CO-DESIGN
(Elective -I)

UNIT –I:
CO-DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
CO-SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II:
PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developmentsin emulation and prototyping architecture specialization techniques, system communicationinfrastructure.
TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture andApplication System classes, Architecture for control dominated systems (8051-Architectures for Highperformance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), MixedSystems.

UNIT –III:
COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies,practical consideration in a compiler development environment.

UNIT –IV:
DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrentcomputations, interfacing components, design verification, implementation verification, verificationtools, interface verification.

UNIT –V:
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System –level specification, design representation for system level synthesis, system levelspecification languages,
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos.
system.

TEXT BOOKS:
1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

DEVICE MODELLING
(Elective -I)

UNIT -I:
INTRODUCTION TO SEMICONDUCTOR PHYSICS: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of modelparameters on structures

UNIT -II:
INTEGRATED DIODES: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small andlarge signal models – SPICE models
Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon modeldynamicmodel, Parasitic effects – SPICE model –Parameter extraction.

UNIT -III:
INTEGRATED MOS TRANSISTOR:NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS deviceequations – Basic DC equations second order effects – MOS models – small signal AC characteristics– MOS FET SPICE model level 1, 2, 3 and 4.

UNIT -IV:
VLSI FABRICATION TECHNIQUES: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V:
MODELING OF HETERO JUNCTION DEVICES: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:
1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:
1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

ADVANCED OPERATING SYSTEMS
(Elective -II)

UNIT –I:
INTRODUCTION TO OPERATING SYSTEMS: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memoryhierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluationof operating System

UNIT –II:
INTRODUCTION TO UNIX AND LINUX: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection,Filters and Editors, Shells and Operations

UNIT –III:
SYSTEM CALLS: System calls and related file structures, Input / Output, Process creation & termination.
Inter process communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams &Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory,Sockets& TLI.

UNIT –IV:
INTRODUCTION TO DISTRIBUTED SYSTEMS: Goals of distributed system, Hardware and software concepts, Design issues.
COMMUNICATION IN DISTRIBUTED SYSTEMS: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Groupcommunication.

UNIT –V:
SYNCHRONIZATION IN DISTRIBUTED SYSTEMS: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm,Atomic transactions
DEADLOCKS: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lockdetection.

TEXT BOOKS:
1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:
1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. G

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN
(Elective -II)

UNIT –I:
ARM ARCHITECTURE:ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts andVector Table, Architecture Revision, ARM Processor Families.

UNIT –II:
ARM PROGRAMMING MODEL – I: Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions,PSR Instructions, Conditional Instructions.

UNIT –III:
ARM PROGRAMMING MODEL – II: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions,Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:
ARM PROGRAMMING: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic,Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:
MEMORY MANAGEMENT: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, AccessPermissions, Context Switch.

TEXT BOOKS:
1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:
1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester 3 1/-/- 3

ADVANCED COMPUTER ARCHITECTURE
(Elective-II)

UNIT -I:
FUNDAMENTALS OF COMPUTER DESIGN: Fundamentals of Computer design, Changing faces of computing and task of computer designer,Technology trends, Cost price and their trends, measuring and reporting performance, Quantitativeprinciples of computer design, Amdahl's law.Instruction set principles and examples- Introduction, classifying instruction set- memory addressingtypeand size of operands, Operations in the instruction set.

UNIT –II:
PIPELINES: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic fivestage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducingpipeline branch penalties.
MEMORY HIERARCHY DESIGN: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtualmemory.

UNIT -III:
INSTRUCTION LEVEL PARALLELISM (ILP) - THE HARDWARE APPROACH: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach,Branch prediction, High performance instruction delivery- Hardware based speculation.
ILP SOFTWARE APPROACH: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelismat compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV:
MULTI PROCESSORS AND THREAD LEVEL PARALLELISM: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain,Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:
INTER CONNECTION AND NETWORKS: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examplesof inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:
1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:
1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain,PeterKacsuk, Pearson Ed.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year I Semester - -/3/- 2

VLSI SYSTEM DESIGN LAB I

MENTOR GRAPHICS / SYNOPSYS / EQUIVALENT CAD TOOLS.

PART I:-VLSI FRONT END DESIGN PROGRAMS:

Programming can be done using any HDL complier, Verification of the Functionality of the moduleusing functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module,Place& Route and implementation of design using FPGA/CPLD Devices.

1.Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, CarryLook Ahead Adder
2.Design of flip flops: SR, D, JK, T
3. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).
4. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
5. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
6. Design of 4- Bit Multiplier and 4-bit Divider.
7. Design of ALU to Perform – ADD, SUB, AND, OR, 1's compliment, 2's Compliment, Multiplicationand Division.
8. Design of Finite State Machine.

PART –II:-VLSI BACK END DESIGN PROGRAMS:

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL orVHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for differenttechnologies, study of secondary effects (temperature, power supply and process corners), Circuitoptimization with respect to area, performance and/or power, Layout, Extraction of parasitics and backannotation, modifications in circuit parameters and layout consumption, DC/transient analysis,Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR Dropanalysis and crosstalk analysis of the following:
CMOS inverter
CMOS NOR/ NAND gates
CMOS XOR and MUX gates
CMOS half adder and full adder
Static / Dynamic logic circuits (register cell)
Latch
Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

LOW POWER VLSI DESIGN

UNIT –I:
FUNDAMENTALS: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation,Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, ShortChannel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, VelocitySaturation, Impact Ionization, Hot Electron Effect.

UNIT –II:
LOW-POWER DESIGN APPROACHES:Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, ArchitecturalLevel Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:
LOW-VOLTAGE LOW-POWER ADDERS: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:
LOW-VOLTAGE LOW-POWER MULTIPLIERS: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:
LOW-VOLTAGE LOW-POWER MEMORIES: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics ofSRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics ofDRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:
1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer,

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

CAD FOR VLSI CIRCUITS

UNIT -I:
VLSI PHYSICAL DESIGN AUTOMATION:VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends inPhysical Design Cycle, Design Styles, System Packaging Styles;

UNIT -II:
PARTITIONING, FLOOR PLANNING, PIN ASSIGNMENT AND PLACEMENT: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm,Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planningalgorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problemformulation, Classification of pin assignment algorithms, General and channel Pin assignments,Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT -III:
GLOBAL ROUTING AND DETAILED ROUTING: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routingalgorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layerrouting algorithms;

UNIT -IV:
PHYSICAL DESIGN AUTOMATION OF FPGAS:FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm forthe Non-Segmented model, Routing Algorithms for the Segmented Model;
PHYSICAL DESIGN AUTOMATION OF MCMS: Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT -V:
CHIP INPUT AND OUTPUT CIRCUITS:ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation andDistribution, Latch-up and its prevention.

TEXT BOOKS:
1. Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:
1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:
SWITCHED CAPACITOR CIRCUITS: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-idealeffects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,biquad filters.

UNIT -II:
PHASED LOCK LOOP (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequencydetector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications

UNIT -III:
DATA CONVERTER FUNDAMENTALS:DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder basedconverters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
NYQUIST RATE A/D CONVERTERS: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/Dconverters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:
OVERSAMPLING CONVERTERS: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Deltasigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:
1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

DESIGN FOR TESTABILITY

UNIT -I:
INTRODUCTION TO TESTING: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trendsaffecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional VersusStructural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:
LOGIC AND FAULT SIMULATION: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithmsfor True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:
TESTABILITY MEASURES:SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and ScanDesign: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
BUILT-IN SELF-TEST: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation,Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BISTSystems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
BOUNDARY SCAN STANDARD: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan TestInstructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSLDescription Components, Pin Descriptions.

TEXT BOOKS:
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:
1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

SCRIPTING LANGUAGES
(Elective -III)

UNIT -I:
INTRODUCTION TO SCRIPTS AND SCRIPTING: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variablesand assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data,Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regularexpressions, Subroutines, Scripts with arguments.

UNIT -II:
ADVANCED PERL: Finger points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the filesystem, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects,Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT -III:
TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow,Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes,Example code.

UNIT -IV:
ADVANCED TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trappingerrors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internetprogramming, Security issues, running untrusted code, The C interface.

UNIT -V:
TK AND JAVASCRIPT: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometrymanagers, PERL-TK.JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script corelanguage, Basic concepts of Pythan.
Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:
1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS:
1. Tcl/Tk: A Developer's Guide- ClifFlynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- WojciechKocjan and PiotrBeltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(Elective -III)

UNIT –I:
INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences.Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems,Digital filters, Decimation and interpolation.
Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sourcesof error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A ConversionErrors, Compensating filter.

UNIT –II:
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, DataAddressing Capabilities, Address Generation UNIT, Programmability and Program Execution, SpeedIssues, Features for External interfacing.

UNIT -III:
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs,Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XXProcessors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals,Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:
ANALOG DEVICES FAMILY OF DSP DEVICES: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, BaseArchitecture of ADSP 2100, ADSP-2181 high performance Processor.Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro SignalArchitecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit,Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface,
Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:
1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran,
Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo,Wiley-IEEE Press, 2007

REFERENCE BOOKS:
1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani andM. Bhaskar, 2002,
TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The ApplicationsEngineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI

5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D.,California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ,ISBN 0750679123, 2005

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

VLSI SIGNAL PROCESSING
(Elective -III)

UNIT -I:
INTRODUCTION TO DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing forLow Power
Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

UNIT –II:
FOLDING AND UNFOLDING: Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimizationin folded architectures – folding of multirate systems
Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT -III:
SYSTOLIC ARCHITECTURE DESIGN: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of SchedulingVector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for SpaceRepresentations contain Delays

UNIT -IV:
FAST CONVOLUTION: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – CyclicConvolution – Design of Fast Convolution algorithm by Inspection

UNIT -V:
LOW POWER DESIGN: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power EstimationApproachesProgrammable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors forMobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:
1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:
1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

MALLAREDDY ENGINEERING COLLEGE
(Autonomous)

M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(Elective-IV)

UNIT –I:
STATISTICAL MODELING: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgromsmodel, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II:
STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, Highlevel statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperatureand power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III:
CONVEX OPTIMIZATION: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis,Generalized geometric programming, geometric programming applied to digital circuit gate sizing,Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomialfitting,Posynomial fitting.

UNIT –IV:
GENETIC ALGORITHM: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design,Layout and Test automation- partitioning-automatic placement, routing technology, Mapping forFPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybridgenetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASPalgorithm-unified algorithm.

UNIT –V:
GA ROUTING PROCEDURES AND POWER ESTIMATION: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-testgeneration procedures, Power estimation-application of GA-Standard cell placement-GA for ATGproblemencoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:
1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - PinakiMazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, LievenVandenberghe, Cambridge University Press, 2004.

MALLA REDDY ENGINEERING COLLEGE
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M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

SYSTEM ON CHIP ARCHITECTURE
(Elective -IV)

UNIT –I:
INTRODUCTION TO THE SYSTEM APPROACH: System Architecture, Components of the system, Hardware & Software, Processor Architectures,Memory and Addressing. System level interconnection, An approach for SOC Design, SystemArchitecture and Complexity.

UNIT –II:
PROCESSORS: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic conceptsin Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing PipelineDelays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions,VLIW Processors, Superscalar Processors.

UNIT –III:
MEMORY DESIGN FOR SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, CacheOrganization, Cache data, Write Policies, Strategies for line replacement at miss time, Types ofCache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC MemorySystem, Models of Simple Processor – memory interaction.

UNIT -IV:
INTERCONNECT CUSTOMIZATION AND CONFIGURATION: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models,Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: Anoverview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design ontoReconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:
APPLICATION STUDIES / CASE STUDIES:SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEGcompression.

TEXT BOOKS:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004,Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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M. Tech (VLSISD) L T/P/D C
I Year II Semester 3 1/-/- 3

SEMICONDUCTOR MEMORY DESIGN AND TESTING
(Elective-IV)

UNIT -I:
RANDOM ACCESS MEMORY TECHNOLOGIES:SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuitoperation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures andtechnologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM,DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM,Advanced DRAM design and architecture, Application specific DRAM.

UNIT -II:
NON-VOLATILE MEMORIES: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gateEPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture,Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:
MEMORY FAULT MODELING TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE:RAMfault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatilememory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing,RAM fault modeling, BIST techniques for memory

UNIT -IV:
SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability,reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), RadiationHardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memorycharacteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level
Radiation Testing and Test structures

UNIT -V:
ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKING TECHNO Logies: FerroelectricRAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimentalmemory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCMtesting and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:
1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K.Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

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M. Tech (VLSISD) L T/P/D C
I Year II Semester - -/3/- 2

MIXED SIGNAL DESIGN LAB

NOTE : Following Experiments must be done using any one of the Back End Tools and all types of Analysis must be carried out(Transient, AC Analysis, DC Analysis, Post Lay out & Pre Layout Simulations etc.)

Minimum 12 Experiments must be conducted

CYCLE 1: ANALOG SIGNAL DESIGN

1. Current Source/Current Mirror Circuits
2. Common Source Amplifier
3. Class AB Amplifier with Load
4. Class AB Amplifier Without Load
5. Feed Back Amplifiers (Any two types among Four)
6. Differential Amplifier (Single Ended)
7. Trans conductance Operational Amplifier
8. CMOS as an Comparator

CYCLE 2: MIXED SIGNAL CIRCUITS

9. Analog Multiplier
10. Switched Capacitor Integrator
11. Switched Capacitor Common Mode Feedback Amplifier
12. Sample and Hold Circuit
13. Digital to Analog Converters (R-2R Ladder/Cyclic)
14. Analog to Digital Converters (SAR/Over Sampling etc)
15. Phase Locked Loop(Beyond the syllabus)